Amendments to the Claims

1. (Currently Amended) A method comprising:

determining a first memory buffer level for at least one memory buffer providing data to digital circuitry,

determining a second memory buffer level for the at least one memory buffer, the second memory buffer level being set greater than the first memory buffer level,

comparing data buffer levels in the at least one memory buffer with the first and second memory buffer levels, and

sending the compared data buffer level to an operating system for the digital circuitry, wherein the operating system causes the ~~switching~~ digital circuitry to switch from a first state to a second state when the compared data buffer level is greater than the second memory buffer level, and wherein the operating system causes ~~switching~~ the digital circuitry to switch from a second state to a first state when the compared data buffer level is less than the first memory buffer level.

2. (Currently Amended) The method of claim 1, ~~further comprising switching~~ wherein the operating system causes the digital circuitry to switch between additional states in response to changing levels of memory buffer data in the at least one memory buffer.

3. (Currently Amended) The method of claim 1, wherein the first and second memory buffer levels are augmented by at least one additional memory buffer level to permit greater switching control by the operating system of the digital circuitry between states in response to compared data buffer levels.

4. (Currently Amended) The method of claim 1, wherein causing the operating system to switch~~ing~~ the digital circuitry between ~~from~~ the first state ~~to~~ and the second state further comprises causing the operating system to adjust~~ing~~ clock frequency of the digital circuitry.

5. (Currently Amended) The method of claim 1, wherein causing the operating system to switch~~ing~~ the digital circuitry between ~~from~~ the first state ~~to~~ and the second state further comprises adjusting voltage of the digital circuitry.

6. (Currently Amended) The method of claim 1, wherein the digital circuitry ~~is~~ comprises a processor, wherein the operating system of the processor directly ~~controlled~~ controls ~~to~~ the switch between states.

7. (Currently Amended) The method of claim 1, wherein the digital circuitry ~~is~~ comprises a processor, wherein the operating system of the processor ~~controlled to~~ controls the switch between states in response to interactions with a power management controller.

8. (Currently Amended) An article comprising a computer-readable medium which stores computer-executable instructions, the instructions defined to cause a computer to:

determine a first memory buffer level for at least one memory buffer providing data to digital circuitry,

determine a second memory buffer level for the at least one memory buffer, the second memory buffer level being set greater than the first memory buffer level,

compare data buffer levels in the at least one memory buffer with the first and second memory buffer levels, and

send the compared data buffer level to an operating system for the digital circuitry, wherein the operating system causes the digital circuitry to switch ~~digital circuitry~~ from a first state to a second state when the compared data buffer level is greater than the second memory buffer level, and wherein the operating system causes the digital circuitry to switch ~~the digital circuitry~~ from a second state to a first state when the compared data buffer level is less than the first memory buffer level.

9. (Currently Amended) The article comprising a computer-readable medium which stores computer-executable instructions of claim 8, wherein the instructions further cause a computer to enable the operating system to switch the digital circuitry between

additional states in response to changing levels of memory buffer data in the at least one memory buffer.

10. (Currently Amended) The article comprising a computer-readable medium which stores computer-executable instructions of claim 8, wherein the instructions further cause a computer to provide augmentation of the first and second memory buffer levels by at least one additional memory buffer level to permit greater switching control by the operating system of the digital circuitry between states in response to compared data buffer levels.

11. (Currently Amended) The article comprising a computer-readable medium which stores computer-executable instructions of claim 8, wherein the instructions further cause a computer to enable the operating system to switch the digital circuitry ~~from~~ between the first state ~~to~~ and the second state by adjusting clock frequency of the digital circuitry.

12. (Currently Amended) The article comprising a computer-readable medium which stores computer-executable instructions of claim 8, wherein the instructions further cause a computer to enable the operating system to switch the digital circuitry ~~from~~ between the first state ~~to~~ and the second state by adjusting voltage of the digital circuitry.

13. (Currently Amended) The article comprising a computer-readable medium which stores computer-executable instructions of claim 8, wherein the ~~instructions further cause a processor in the~~ digital circuitry ~~of the computer to~~ comprises a processor, wherein the operating system of the processor directly controls the switch between states.

14. (Currently Amended) The article comprising a computer-readable medium which stores computer-executable instructions of claim 8, wherein the ~~instructions further cause a processor in the~~ digital circuitry ~~of the computer~~ comprises a processor, wherein the operating system of the processor ~~to be controlled to~~ controls the switch between states in response to interactions with a power management controller.

15. (Currently Amended) A power reduction system comprising:

a memory buffer monitoring unit to compare a memory buffer level to a first and a second memory buffer level for at least one memory buffer providing data to an operating system for digital circuitry, the second memory buffer level being set greater than the first memory buffer level, and

a switching unit controlled by the operating system to adjust digital circuitry state, moving from a first state to a second state when a compared data buffer level in the memory buffer monitoring unit is greater than the second memory buffer level, and moving from a second state to a first state when the compared data buffer level is less than the first memory buffer level.

16. (Currently Amended) The system of claim 15, further comprising enabling the operating system to switch~~ing~~ the digital circuitry between additional states in response to changing levels of memory buffer data in the at least one memory buffer.

17. (Currently Amended) The system of claim 15, wherein the first and second memory buffer levels in the memory buffer monitoring unit are augmented by at least one additional memory buffer level to permit greater switching control by the operating system of the digital circuitry between states in response to compared data buffer levels.

18. (Currently Amended) The system of claim 15, wherein the ~~digital circuitry controlled by the~~ switching unit controlled by the operating system can ~~be~~ adjust~~ed~~ the digital circuitry between ~~from~~ the first state ~~to~~ and the second state by the switching unit changing clock frequency of the digital circuitry.

19. (Currently Amended) The system of claim 15, wherein the ~~digital circuitry controlled by the~~ switching unit controlled by the operating system can ~~be~~ adjust~~ed~~ ~~from~~ between the first state ~~to~~ and the second state by the switching unit changing voltage of the digital circuitry.

20. (Currently Amended) The system of claim 15, wherein the digital circuitry ~~controlled by the switching unit is~~ comprises a processor, wherein the operating system of the processor directly ~~controlled to~~ controls the switch between states.

21. (Currently Amended) The system of claim 15, wherein the digital circuitry ~~controlled by the switching unit is~~ comprises a processor, wherein the operating system of the processor ~~controlled to~~ controls the switch between states in response to interactions with a power management controller.

22. (New) The system of claim 15, wherein the switching unit controlled by the operating system can adjust between the first state and the second state by the switching unit changing voltage and clock frequency of the digital circuitry.

23. (New) The article comprising a computer-readable medium which stores computer-executable instructions of claim 8, wherein the instructions further cause a computer to enable the operating system to switch the digital circuitry between the first state and the second state by adjusting voltage and clock frequency of the digital circuitry.

24. (New) The method of claim 1, wherein causing the operating system to switch the digital circuitry between the first state and the second state further comprises adjusting voltage and clock frequency of the digital circuitry.